Abstract of the Disclosure

First-in/first-out ("FIFO") memory circuitry includes first and second Gray-code-based counters for respectively counting write and read clock signals. A Gray code subtractor subtracts from one another the counts output by the counters. Shift register circuitry shifts in successive data words in synchronism with the write clock signal. The shift register circuitry includes selection circuitry configured to select one of the data words based on a Gray code decoding of information from the subtractor. Circuitry may also be included to monitor the information from the subtractor to detect full or empty conditions of the shift register circuitry.